CLAIMS

1. An apparatus for testing a semiconductor die which comprises:

(a) a package having a cavity therein;

(b) a plurality of terminals in said package disposed at the periphery of said cavity;

(c) a semiconductor die to be tested having a plurality of bond pads thereon, said die disposed in said cavity;

(d) an interconnecting layer having electrically conductive paths thereon disposed in said cavity, each of said paths having first and second spaced apart regions thereon, said first region of each path being aligned with and contacting a said bond pad; and

(e) an interconnection between said second spaced apart region of each of said paths and one of said plurality of terminals.

2. The apparatus of claim 1 wherein said second spaced apart region of each of said paths is a bump aligned with and contacting one of said plurality of terminals.

3. The apparatus of claim 1 further including a compliant layer disposed over said interconnecting layer and providing a force causing engagement of at least said first spaced apart regions and said bond pads.

4. The apparatus of claim 2 further including a compliant layer disposed over said interconnecting layer and providing a force causing engagement of at least said first spaced apart regions and said bond pads.

5. The apparatus of claim 1 wherein said first region is a compliant bump probe tip having a first predetermined height above said layer, further including a standoff on said layer having a second predetermined height above said layer less than said first height.

6. The apparatus of claim 2 wherein said first region is a compliant bump probe tip having a first predetermined height above said layer, further including a standoff on said layer having a second predetermined height above said layer less than said first height.

7. The apparatus of claim 3 wherein said first region is a compliant bump probe tip having a first predetermined height above said layer, further including a standoff on said layer having a second predetermined height above said layer less than said first height.

8. The apparatus of claim 4 wherein said first region is a compliant bump probe tip having a first predetermined height above said layer, further including a standoff on said layer having a second predetermined height above said layer less than said first height.

9. An interconnecting layer for use in a semiconductor package which comprises;

(a) an electrically insulating layer;

(b) electrically conductive paths on said layer, each of said paths having first and second spaced apart regions thereon, said second spaced apart region of each of said paths being a compliant bump having a height greater than all other structures on said layer; and

(c) a standoff disposed on said layer and having a height less than said bump.

10. The layer of claim 9 wherein said second region is a bump extending above the level of said electrically conductive path.

11. The layer of claim 9 wherein said layer is formed of silicon.

12. The layer of claim 10 wherein said layer is formed of silicon.

13. The layer of claim 9 wherein said layer is flexible.

14. The layer of claim 10 wherein said layer is flexible.

15. The layer of claim 11 wherein said layer is flexible.

16. The layer of claim 12 wherein said layer is flexible.

17. A method of testing a semiconductor chip which comprises the steps of:

(a) providing a package having a cavity therein and a plurality of terminals in said package disposed at the periphery of said cavity;

(b) disposing a semiconductor die to be tested having a plurality of bond pads thereon in said cavity;

(c) disposing an interconnecting layer having electrically conductive paths thereon in said cavity wherein each of said paths has first and second spaced apart regions thereon, and aligning said first region of each path being aligned and contacting a said bond pad; and

(d) interconnecting said second spaced apart region of each of said paths and one of said plurality of terminals.

18. The method of claim 17 wherein said second spaced apart region of each of said paths is a bump aligned with and contacting one of said plurality of terminals.

19. The method of claim 17 further including a compliant layer disposed over said interconnecting layer and providing a force causing engagement of at least said first spaced apart regions and said bond pads.

20. The method of claim 18 further including a compliant layer disposed over said interconnecting layer and providing a force causing engagement of at least said first spaced apart regions and said bond pads.

21. The method of claim 20 wherein said first region is a compliant bump probe tip having a first predetermined height above said layer, further including a standoff on said layer having a second predetermined height above said layer less than said first height.